METHOD FOR CREATING HDL DESCRIPTION FILES OF DIGITAL SYSTEMS, AND SYSTEMS OBTAINED

This invention relates firstly to the technical domain of computer-aided design (CAD) of integrated digital electronic systems also called "electronic chips", and secondly the technical domain of the electronic chips obtained.

5   In general, the design of complex electronic systems to be integrated on the same electronic chip uses a phase in which a description of the integrated electronic system is generated in a so-called High level Description Language (HDL) at a so-called Register Transfer Level (RTL). The languages

10   used most frequently to make such an HDL description are the Verilog or VHDL languages, although it must not be assumed that these are the only languages that can be used to produce an HDL description of a digital integrated electronic system at the RTL level.

15   The description of an integrated electronic system in HDL language is usually materialised in the form of a system of electronic files or description database that can then be composed of a single text file produced in an HDL language, or otherwise it may include several description text files, some

20   of the files corresponding to the particular description of modules or parts of the integrated system, while other files describe the interaction and relations between the different modules and links existing between them.

To obtain a description of the electronic chip that could

25   be qualified as physical with relation to the HDL language description that could be qualified as being functional or behavioral, a synthesis or compilation is made from the system of HDL description files using a computer tool usually called a silicon compiler that is used to obtain a hardware

30   description at logic gates as a function of the selected technology, description also called a "netlist" that will then

be used to obtain a physical representation of the integrated electronic system in the form of masks used for manufacturing the chip in accordance with the different known techniques that do not form part of the scope of this invention.

5   An integral digital electronic system thus obtained must obviously enable guaranteed reliability and operation in accordance with the target set during its design.

Thus, it appeared necessary to provide systems or means for verifying perfect operation of an electronic system during
10   its design, obviously in an automated manner, either using external devices that will be connected to the integrated electronic system once it has been manufactured, or using test systems forming an integral part of the integrated electronic system obtained.

15   In general, such an approach oriented towards testability of integrated electronic systems, is qualified as a DFT (Design For Test) technique: and more particularly the term BIST 'Built-in Self-test) is used when it is intended to build in its own automatic test means into the integrated electronic
20   system.

A first approach to verify correct operation of the integrated digital electronic system consists firstly of verifying perfect operation of memory elements or flip-flops within the built-in system that will temporarily store
25   intermediate processing results or signal values. This invention relates to local memory elements present within so-called sequential components. These sequential components represent most complex built-in circuits such as microprocessors or signal processing processors. Since a
30   sequential circuit is composed of combinational logic elements and sequential elements or flip-flops, to be distinguished from memory elements of RAM or ROM memory modules.

Testing of sequential circuits includes a step to generate test patterns using special purpose software tools called ATPG for "Automatic Test Pattern Generators". The quality of the test patterns generated determines the test phase after manufacturing and the capacity of test patterns to reveal the presence of defects. The generation of quality test patterns requires the use of DFT techniques such as the SCAN. The "SCAN" technique consists of chaining the different memory elements to each other so as to obtain one or several SCAN chains that will be activated within the scope of operation of the integrated circuit in test mode.

Memory element SCAN and chaining functions can be put into place in the hardware description (netlist) of the integrated digital electronic circuit as described in patent US 6 311 317. However, in particular, considering the very large number of logic gates, this insertion done automatically or semi-automatically requires a very long calculation time. Furthermore, this insertion can disturb operation of the integrated electronic logic system in normal mode, such that after elements have been chained at the netlist hardware description, it may be necessary to modify the design of the circuit and therefore to rewrite the description of the circuit in the HDL language, before making a new silicon compilation and a new insertion of the chaining of memory elements in the netlist.

This iterative process can be very long and consume hardware and human resources, and forms an obstacle to a reduction in the time necessary to design reliable and high performance integrated electronic systems.

Thus, it appeared that if SCAN functions can be integrated at the HDL description before the synthesis phase, it would be possible to substantially reduce the design time for the integrated electronic system.

Thus, another method has been proposed consisting of building in functions called chaining or SCAN functions at the RTL level, within the framework of the HDL description of the integrated digital electronic system.

5   For example, patent US 6 256 770 proposed a method and device for implementing a test function of an integrated electronic system within the framework of its description in the HDL language. This patent firstly describes the assignment of portions of memory element chains to different

10   modules in the circuit, followed by scheduling of these portions of memory element chains based on an analysis of functional relations existing between memory elements or data patterns in the HDL descriptions of modules. The next step based on this schedule is to insert chaining instructions in

15   the description of the module concerned in the HDL language so that, during synthesis of the said module, the integrated digital electronic system incorporates the logical electronic circuits necessary for the test resulting from such chaining, for each module concerned.

20   Such a method and device enable automatic insertion of HDL instructions so that when the circuit is synthesised, SCAN functions can be obtained so as to generate good quality test patterns for the integrated circuit under test.

However, in practice, it has been found that the step to

25   analyse functional relations between the different data patterns, within the framework of the design of particularly complex integrated digital electronic systems, requires a particularly long calculation time such that the benefits of insertion of SCAN functions at the RTL level in the HDL

30   language are reduced or even completely cancelled out due to the calculation time or calculation power necessary to make this insertion in accordance with US patent 6 256 770.

Patent application US 2003/0023941 discloses another manner of automatically inserting instructions in the HDL language at the RTL, to implement SCAN functions in the integrated electronic system that will be obtained by a synthesis of the HDL description thus modified. According to this document, SCAN chains and test points are inserted in the HDL language at the RTL level firstly by analysing the testability of the description of the integrated electronic system in the HDL language.

Although the method described in US application 2003/0023941 does enable automatic insertion of HDL instructions corresponding to SCAN functions after synthesis, the testability analysis is a step that consumes large quantities of calculation resources or time such that the gains obtained due to automatic modification of the integrated electronic system at the HDL level are minimised due to the testability analysis calculation times.

Furthermore, US application 2003/0023941 also discloses how SCAN chains can be inserted by making an identification and an analysis of the different existing clock domains followed by a calculation to minimise test generation costs and to minimise clock domains. This analysis of clock domains and this minimisation also require large resources.

Therefore, there is a need for a method that automatically inserts SCAN functions within the framework of the HDL description at the RTL level of an integrated digital electronic system, to substantially reduce calculation times, while offering an integrated digital electronic system that, after synthesis, will have performances at least equivalent to the performances of integrated systems that would be synthesised, at RTL level, from HDL descriptions processed by methods according to prior art.

In order to achieve this purpose, the invention relates to a method for analysing a set of original description files for an integrated digital electronic system in a description language called the HDL language at the register transfer

5   level, in order to automatically insert instructions in the HDL language into description files to obtain a new set of description files in the HDL language for the integrated digital electronic system including test functions such that during automatic synthesis of the integrated digital

10 electronic system using a new set of HDL description files, the integrated digital electronic system obtained builds in at least some of the logical electronic circuits necessary to test operation of at least the memory elements.

According to the invention, the analysis and automatic

15 insertion method is characterised in that it includes the following steps:

   • automatic localisation of HDL instructions or instruction sequences that during synthesis of the system, will be at the origin of the memory elements,

20   in the original HDL description files;

   • automatic and sequential insertion in at least part of HDL description files, and without relational or functional analysis of the identified memory elements, of HDL instructions used to obtain firstly

25   at least one so-called "SCAN" chain connecting the memory elements, and secondly means of implementing the so-called SCAN test of the circuit, during synthesis of the system.

According to the invention, the set of HDL description

30 files of an integrated digital electronic system includes one or several text or ASCII code files that describe one, several or all functional modules of the integrated digital electronic system and any relations existing between the different

modules, in HDL instructions. According to the invention, the HDL description of the integrated digital electronic system may also be described within the framework of a description database.

5 Similarly, for the purposes of the invention, all HDL instructions necessary to use the so-called SCAN test are inserted, namely particularly the insertion of instructions used to put the circuit to be tested into test mode, test signal input instructions, test signal output instructions,
10 instructions for implementing a test clock, instructions for chaining memory elements and instructions for definition of a SCAN test controller, although this list cannot be considered to be exhaustive or exclusive of other functions that might be necessary for implementing the SCAN test.

15 The method according to the invention has the advantage that it does not require any large calculation resources due to the sequential insertion of element chaining instructions as they appear in HDL description pages (i.e. without analysing any relations between them) such that the method
20 according to the invention can be used on a computer such as a personnel computer while resulting in shorter processing times than are necessary for using methods according to prior art.

The inventors have demonstrated that there was no need to carry out a relational or functional analysis, or even a
25 testability analysis to insert HDL instructions necessary for implementing SCAN functions and that a sequential insertion of the said HDL instructions, that could be qualified as being a heuristic insertion, as these instructions that could generate memory elements appear in HDL description files, finally makes
30 it possible to obtain all functions to test memory elements of the integrated digital electronic system without modifying performances or excessively increasing the surface area of these memory elements.

The invention also relates to an integrated digital electronic system resulting from the synthesis of a set of description files in the HDL language obtained by use of the method according to the invention and including at least part of the logical electronic circuits necessary to test at least operation of the memory elements such as one or several SCAN chains.

According to one characteristic of the invention, the analysis and automatic insertion method includes a step to record the new set of HDL description files obtained.

According to another characteristic of the invention, in order to prevent violations to SCAN rules during synthesis of the circuit using the new set of HDL description files, the analysis and automatic insertion method includes a step to identify the different existing clock domains, and the step to insert HDL memory element chaining instructions is then carried out so as to create at least one distinct SCAN chain for each clock domain.

Furthermore according to the invention, the dimension of variables or signals is determined before the step to insert HDL SCAN instructions so as to implement the SCAN at the RTL level that guarantees that SCAN rules will be respected during the synthesis. Thus for example, in the case of integer or enumeration type VHDL variables, the invention requires that the length of words corresponding to the number of bits should be fixed before VHDL SCAN instructions are inserted, so as to guarantee that elementary memories from which each memory is composed are correctly chained to each other.

Thus, according to another characteristic of the invention, the analysis and automatic insertion method:

- includes a step to analyse or index all original HDL description files and to create at least one indexing file comprising the list of design units if there are

any (entity, library, packet) for each HDL object and process, all declarations for each design unit, each declaration comprising the line number, the object name, its type, its size and the associated type of test construction,

- and the step to localise HDL instructions that will be at the origin of memory elements during synthesis of the circuit, includes a phase to create a memory localisation file comprising at least the name of the HDL object corresponding to each memory element, with its type, dimension and coordinates in the original HDL description files.

Furthermore, since information about the dimension of some variables could be missing in the set of original HDL description files, a preferred embodiment of the invention includes a step either for an automatic definition of this dimension based on a predetermined default value, or in which a user of the method makes the definition interactively.

Similarly, and according to a preferred variant embodiment, the method according to the invention checks compatibility between memory elements when HDL chaining instructions are inserted. In fact, it is only possible to chain memory elements corresponding to objects of the same type and with a compatible dimension. Thus, if there is an incompatibility, the invention includes a preferred but not strictly necessary method of inserting HDL chaining instructions including either a phase for automatic transformation of the type and / or dimension of one of the two objects at the origin of the conflict, or a phase in which the user interactively modifies the type and / or the dimension of one of the two objects at the origin of the conflict. Refer to patent application US 2003/0033595 for information about automatic detection and correction of such

conflicts corresponding to syntax or grammatical errors in the use of the language.

According to another characteristic of the invention, the HDL instruction insertion step for chaining of memory elements includes:

- a phase to insert HDL instructions for local chaining of memory elements at the set of HDL instructions corresponding to an HDL process so as to obtain at least one distinct chain of memory elements for each HDL process during the synthesis,

- a phase to insert HDL chaining instructions, called global chaining, at the HDL description files, so as to obtain at least one chain of memory elements during the synthesis comprising the chains of memory elements created during the local chaining phase.

In general, the term chaining in the sequential domain is used for chaining within processes, while the term chaining in the concurrent domain is used for chaining external to processes.

Thus, according to another characteristic of the invention, the step for automatic insertion of HDL instructions includes the following phases:

- insertion of HDL instructions corresponding to test signals used as an input-output port,

- insertion of HDL instructions corresponding to intermediate work signals, in the case of memory elements between several processes involving primary input/output ports,

- insertion of HDL instructions in each process, so as to obtain at least one so-called "SCAN" chain during synthesis of the circuit, connecting memory elements specific to the process,

- insertion of HDL instructions providing concurrent assignment of input and output chains of SCAN chains external to processes.

According to the invention, the method of analysing and inserting HDL instructions may be used within the framework of different HDL description languages such as Verilog or VHDL, it being understood that these are non-limitative examples and that the process according to the invention can be used for other HDL description languages.

Furthermore, the process can also be used on a heterogeneous set of original HDL language description files for example but not exclusively comprising some description files produced in the Verilog language and other description files produced in the VHDL language.

Thus, according to another characteristic of the invention, when Verilog and VHDL languages are used as HDL description languages, the step to localise HDL instructions at the origin of memory elements includes:

- a step to search for synchronised processes to detect objects assigned within these processes,
- application of the following rules for identification of instructions at the origin of memory elements:
  - any object assigned within one process and that is read in another process or in the concurrent part of the HDL code will be considered as being a memory element,
  - in a synchronised process, any object assigned within one branch of an "if" control structure without being assigned within all other branches of this same structure is considered to be a memory element,

* in a synchronised process, any object that is read before it is written is considered to be a memory element.

In one preferred embodiment of the process according to the invention and within the framework of local chaining of a process described in the VHDL language, a phase is included to insert VHDL instructions for the definition of intermediate signals designed to reuse values of chains of variable strings, to enable assignment and chaining of these chains external to the processes.

Furthermore, according to the invention, automatic insertion of HDL instructions must be done in such a way as to not induce any functional degradation of the code of the original integrated digital electronic system in the HDL language.

According to another characteristic of the invention, programmable SCAN chains are created so as to enable optimisation of SCAN chains and an improvement to the coverage of faults after synthesis of the integrated digital electronic system using the new set of HDL description files without it being necessary to modify the description in the HDL language again and to use the process according to the invention again, and thus to prevent an increase in the circuit design time. To achieve this, the step to insert HDL SCAN instructions includes a phase to insert HDL instructions that will generate a programmable multiplexer during the synthesis inserted between at least some of the memory elements of a SCAN chain. Preferably, such a multiplexer is inserted between all successive memory elements of the SCAN chains. Obviously, HDL instructions corresponding to a controller of the multiplexers inserted in SCAN chains are also inserted.

It should be noted that the different characteristics of the method according to the invention like those described

above may be combined in different combinations when these characteristics are not incompatible with each other.

The invention also relates to an integrated digital electronic system or single chip system that includes at least one functional combinational logic module and associated memory elements and SCAN type test means including at least one chain of memory elements. According to the invention, the integrated digital electronic system is characterised in that it includes means for programmable reconfiguration of the SCAN chain.

According to another characteristic of the invention, once again so as to improve the test capacities of the circuit that will be obtained from the new HDL description file set, the process includes a step to insert HDL instructions which will be synthesized to create built-in system tests (BIST) of the integrated digital electronic system. Such means include at least one automatic Test Pattern Generator (TPG), means of analysing the response of the electronic system and the test control means. According to one preferred characteristic of the invention, the automatic test pattern generator includes a linear Parallel Random Pattern Generator (PRPG) and is designed such that the initialisation sequence of the parallel random pattern generator is programmable. Furthermore, according to one preferred embodiment of the invention, the test pattern generating structure and the response analysis structure are based on the programmable or reconfigurable SCAN structure mentioned above.

The different characteristics of an integrated digital system according to the invention as mentioned above may be combined with each other according to different combinations when these characteristics are not incompatible with each other.

The invention also relates to an automated design device in a description language at the register transfer level, called the HDL language, of a complete system or part of an integrated digital electronic system, this device comprising

5   at least one calculation unit, a memory unit and a file storage unit, characterised in that the storage unit includes HDL language description files of the system or part of the integrated electronic system and in that the calculation and memory units are adapted to generate new HDL description files

10   of the system or part of this system that include HDL descriptions, using the method according to the invention and starting from HDL description files, such that the system or part of the integrated digital electronic system obtained from the new files includes at least part of the electronic logic

15   circuits necessary for the operational test of at least the memory elements.

In one preferred embodiment, the device includes a personal computer using a program which is executed to use the process according to the invention.

20   The invention also relates to a data support that can be read by the computer on which a program is recorded, which when executed by a computer enables use of the method according to the invention.

Various other characteristics of the invention will

25   become clear from the following description made with reference to the appended drawings that show different purposes of the invention in non-limitative forms provided as examples.

Figure 1 shows an example flowchart for use of the method

30   according to the invention.

Figure 2 shows an original description file of a portion of an integrated digital system, in the VHDL language.

Figure 3 shows an example file generated during use of the method according to the invention, on the file in **Figure** 2.

Figure 4 shows an original description file of a portion of an integrated digital system, in the Verilog language.

Figure 5 shows an example file generated during use of the process according to the invention, on the file in **Figure** 4.

Figures 6 **and** 7 show examples of indexing files of memory elements generated by the method according to the invention for files according to **Figures** 2 **and** 4.

Figures 8 **and** 9 show HDL description files corresponding to the original files in **Figures** 2 **and** 4 respectively, incorporating HDL SCAN instructions automatically inserted by the method according to the invention.

Figure 10 diagrammatically shows use of means of reconfiguring SCAN chains of an integrated digital system.

Figure 11 diagrammatically shows an integrated digital system like that obtained after synthesis of an HDL description generated by the process according to the invention and using built-in self-test "BIST" functions.

As previously mentioned, a first embodiment of the method according to the invention is intended to insert an HDL instruction circuit at the HDL language description, that after synthesis of the circuit will provide the circuit with all means necessary to test at least part of its memory elements using the SCAN technique. The invention is intended to achieve this purpose without making any prospective analysis of the circuit such as a relational or functional analysis requiring expensive calculation resources and introducing long processing times. On the other hand, according to the invention, instructions corresponding to SCAN chains and associated functions are inserted as memory

elements or HDL instructions corresponding to memory elements occur. Obviously, according to the invention, this chaining is done by testing that the SCAN chain(s) being produced satisfy criteria imposed by the user if any, while progress is

5 being made, and any necessary corrections are made by taking action on the chains and / or chain segments already produced.

In one preferred embodiment, the method according to the invention shown in the flowchart in Figure 1, includes firstly a step 1 for automatic localisation of the instructions that

10 will be at the origin of memory elements during synthesis of the system.

This automatic localisation may involve several phases and in one preferred embodiment, the automatic localisation step includes a step **1a** for analysis or indexing of all

15 original description files in order to create at least one **VIF** indexing file containing the list of design units if they exist (entity, library, packet), and all declarations for each design unit, each declaration including the line number, the object name, type, size and the associated control

20 construction type. This indexing file will then contain at least the type and coordinates in the original or initial HDL description files, for each HDL object and process.

A **VIF** indexing file like that shown in **Figure 3** is generated within the framework of this analysis or indexing

25 step 1a for example done starting from a description file for a process in the VHDL language like that shown in **Figure 2**.

According to the invention, this analysis or indexing step **1a** may be carried out for other types of HDL language. Thus, **Figure 4** shows an example original or initial

30 description file in the VERILOG language based on several processes and the indexing step **1a** applied to this file will be used to obtain a VIF indexing file like that shown in **Figure 5**.

It should be noted that according to the invention, the indexing step 1a may lead to the creation of several indexing files, an indexing file system and preferably but not strictly necessarily, the creation of an indexing database.

Within the framework of the indexing step, the method according to the invention includes indexing of identical instances that might be present in the HDL description of the system, in addition to indexing of the different elementary instructions. Identical instances means a single file or a single set of HDL files describing the part of the system that is used several times in the system.

After this indexing step **1a**, there is a step **1b** for automatically localising HDL instructions that will be the origin of memory elements after synthesis of the circuit. According to the invention, this localisation step **1b** is used for the different types of HDL description language, for example but not exclusively VHDL and Verilog languages that may also be used in combination to describe a single system. Some parts of this system may thus be described by files written in the VHDL, while other parts of the system are described by files written in Verilog.

In its preferred embodiment and for use in VHDL or Verilog files, the step **1b** for localising HDL instructions at the origin of memory elements includes a step to search for synchronised processes so as to detect objects assigned within these processes. This step to search for synchronised processes is made from the result of the indexing step 1a, namely by processing of **VIF** Files or data from the database created or defined during this step **1a** and possibly by processing of the initial **HDL** description files for the system, in the HDL language. After localisation of the synchronised processes, instructions that might generate

memory elements during synthesis are identified using the following rules:

- any object assigned within one process and that is read in another process or in a concurrent part of the HDL code will be considered as being at the origin of a memory element and

- in a synchronised process, any object assigned within one branch of an "if" control structure without being assigned within all the other branches of this structure is considered as being at the origin of a memory element;

- in a synchronised process, any object that is read before being written is referenced as being at the origin of a memory element.

The step to identify the localisation step **1b** is carried out using the result of the indexing step **1a**, like the step to search for synchronised processes, namely by a processing of **VIF** Files or data in the database created or defined during this step **1a** and possibly by processing of initial HLD description Files for the system, in the HDL language. The localisation step **1b** also includes a step to write or create a MEM File that lists at least the name of the corresponding HDL object and its type, dimension and coordinates in the original HDL description files, for each memory element. **Figure 6** shows the localisation file for MEM File memory elements obtained for the HDL description file in the VHDL language according to **Figure 2**, by processing of the VIF indexing File in **Figure 3**. Similarly, **Figure 7** shows the localisation file for MEM File memory elements obtained for the HDL description File in the Verilog language according to **Figure 4** by processing of the VIF indexing File in **Figure 5**. Obviously, according to the invention, the step to create one or a set of localisation files such as the MEM Files may equally apply to

the creation of a database and to filling in a database with information on each memory element as listed non-limitatively above.

Another purpose of the invention is to overcome the lack of a certain amount of information related to the dimensions of some original HDL description file variables by including either a step to automatically choose the value of the missing dimension based on a default value predetermined by the user before or during use of the process according to the invention, or an interactive definition step with the user of the method as this lack of information occurs, depending on the choice of the user. The values of the dimensions thus defined are then recorded in MEM localisation Files or in the corresponding database(s).

According to one essential characteristic of the invention, the method includes an insertion step 2 to insert HDL instructions in at least part of the original HDL description file(s) of the system in the HDL language, after the localisation of HDL instructions that will be at the origin of memory elements during the synthesis, , and during synthesis of the system, these instructions will be used to obtain at least one SCAN chain, and means of performing the SCAN test, for example but not exclusively such as SCAN inputs and outputs, means of putting the system into test mode, a SCAN test clock and a SCAN test controller.

HDL instructions for the SCAN will be inserted so as to prevent any violation of SCAN rules during synthesis of the circuit. The method according to the invention will then preferably include a phase to identify any different existing clock domains accompanied by a record in the files or the ad-hoc localisation database of the different clock domains, if applicable.

Preferably, the step 2 to insert HDL SCAN instructions is done as a function of parameters fixed by the user, namely the number and length of SCAN chains for the entire system or for some elements of the systems concerned.

5   Thus, the insertion step 2 will use the result of the localisation step 1 such as the MEM File, the original HDL description files, localisation of the different clock domains and SCAN usage parameters defined by the user.

According to the invention, HDL memory element chaining
10   instructions are inserted locally at first and then globally.

The local chaining phase, repeated as many times as necessary, relates to the insertion of HDL chaining instructions at the overall HDL instruction level corresponding to an HDL process, so as to obtain at least one
15   chain of memory elements for each HDL process, during the synthesis. In this respect, within the framework of local chaining of a process described in the VHDL language, the invention includes a phase to insert VHDL definition instructions for intermediate signals designed to reuse
20   variable chains so as to enable their assignment and chaining outside processes.

Thus according to one preferred embodiment of the invention, the phase for automatic insertion of HDL instructions for local chaining includes the following phases:
25   • insertion of HDL instructions corresponding to test signals used as an input-output port,
• possible insertion of HDL instructions corresponding to intermediate work signals,
• insertion of HDL instructions in each process, to
30   obtain at least one chain called the "SCAN" chain during synthesis of the circuit, linking the memory elements specific to the process,

- insertion of HDL instructions for concurrent assignment of input and output chains of the SCAN chains external to processes.

It should be noted that in order to respect SCAN rules, the invention requires a verification of the compatibility of memory elements with each other when HDL chaining instructions are inserted, and to achieve this, the step to insert HDL chaining instructions includes either a phase for automatic transformation of the type and / or dimension of one or both objects at the origin of the conflict, or an interactive modification phase with the user of the type and / or dimension of one or both of the objects at the origin of the conflict.

Global chaining occurs after local chaining, and includes a phase repeated as many times as necessary to insert an HDL global chaining instructions in the HDL description files so as to obtain at least one chain of memory elements during the synthesis, comprising memory element chains created during the local chaining phase.

Thus, when the method according to the invention is used, the result is the SCANNED HDL File shown in Figure 8, produced from the original VHDL HDL file shown in Figure 2, containing a VHDL description of the same system containing VHDL instructions that will be at the origin of the SCAN functions during the synthesis. Similarly, Figure 9 shows the Verilog Scanned HDL description File obtained by use of the process according to the invention on the original Verilog description file as shown in Figure 4.

It should be noted that the method according to the invention is preferably used so as to take account firstly of the existence of identical instances such as instances indexed during the indexing step 1a, and secondly the user's choices that may for example result in an instance in part of the

system being concerned by a single SCAN chain, while the same instance in another part of the system is concerned by several SCAN chains, it being understood that these two or multiple identical instances should be described by the same file or set of HDL files. The invention thus proposes to satisfy this requirement by modifying the instance by automatic insertion of SCAN HDL instructions when it appears for the first time during automatic insertion of SCAN HDL instructions for the set of system description files. Then, whenever the said instance is encountered again, a check is made that the SCAN HDL instructions can be used to satisfy local SCAN constraints, and if this is the case no modification is made to description files of the instance. On the other hand if this is not the case, the description file(s) of the instance is (are) modified and all previous locations in which the said instance occurred are verified and its environment is modified so as to satisfy local SCAN constraints with the new form of the instance. This method of proceeding, in accordance with the spirit of the invention, avoids any predictive analysis calculation on identical instances and reconsiders insertions of HDL instructions already made, only when necessary.

In one variant embodiment of the method, the invention proposes to enable a designer to change his mind about the choice related to the configuration of SCAN chains that are built at RTL level. To achieve this, the invention proposes to insert HDL reconfiguration instructions in addition to SCAN HDL instructions, namely firstly HDL instructions that define intermediate switches inserted between each memory element of a SCAN chain and / or between parts of SCAN chains, and secondly HDL instructions corresponding to at least a controller of these intermediate switches.

HDL SCAN and reconfiguration instructions will be used to make an integrated digital system S with functions like those

schematically shown in Figure 10, during synthesis. Thus, the system S includes SCAN chain portions 11, 12, 13, 14 connected to each other one after the other as shown in Figure 10, by intermediate switches 15, 16 connected to a controller 17.

5 In using these means, it becomes possible to dynamically reconfigure SCAN chains after synthesis at hardware level by redefining the following parameters:

➢ size of SCAN chains

➢ physical configuration of one or several SCAN chains.

10 As shown in Figure 10, such a reconfiguration requires a controller 17 that acts on the switches 15, 16 to activate connections of portions of chains 11 to 14 to each other and with the controller 17 depending on the configuration sequence activated at the controller.

15 In one embodiment, the invention also includes a step for automatic insertion of HDL instructions into the HDL description files of the system, and after synthesis of the system these HDL instructions will provide it with all Built-In Self-Test (BIST) functions.

20 Thus, the invention includes a step to automatically insert built-in HDL self-test instructions that will be at the origin of at least the following during the synthesis:

- test pattern generation means such as a test pattern generator 20,

25 - means of analysing the response of the tested circuit such as a test result compression block 21,

- test control means such as a test controller 22,

- a test input 23 and output 24.

As shown in Figure 11, these elements relate to the 30 circuit 25 to be tested that can perform all or only part of the functions of the system S.

According to the invention, the test controller will be adapted to enable at least programming of the initialisation

sequence or sequences of the test generator so as to increase the reliability of the built-in self-test and particularly fault coverage. The test controller will be adapted to enable programming of the test controller configuration and possibly

5   programming of the SCAN controller, ion order to further increase the fault coverage.

According to another characteristic of the invention, there is a step after the synthesis to program the test controller and possibly the SCAN controller, this programming

10   can then be made at a low level on the test controller so as to fix its test parameters.

Obviously, various modifications to the invention can be made without going outside its scope.